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DISTRIBUTED GENERATION SYSTEM USING PV CELLS BASED ON HIGH STEP-UP DC–DC CONVERTER

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Abstract- *In this paper, a novel high stride up dc–dc converter for circulated era frameworks is proposed with pv cells. The inverter is the heart of the PV system and is the focus of all utility-interconnection codes and standards. A Solar inverter or PV inverter is a type of electrical inverter that is made to change the direct current (DC) electricity from a photovoltaic array into alternating current (AC) for use with home appliances and possibly a utility grid. The idea is to use two capacitors and one coupled inductor. The two capacitors are charged in parallel amid the switch-off period and are released in arrangement amid the switch-on period by the vitality put away in the coupled inductor to accomplish a high stride up voltage pick up. Likewise, the spillage inductor vitality of the coupled inductor is reused with an aloof cinch circuit. In this way, the voltage weight on the fundamental switch is lessened. The switch with low resistance RDS (ON) can be embraced to decrease the conduction misfortune. What's more, the converse recuperation issue of the diodes is lightened, and consequently, the effectiveness can be further made strides. The working rule and relentless state investigations are talked about in subtle element. At last, a model circuit with 24-V data voltage, 400-V yield voltage, and 200-W yield force is actualized in the research center to confirm the execution of the proposed converter.*

Index Terms—Coupled inductor, distributed generation (DG) system, high step-up.

INTRODUCTION

In recent years, distributed generation (DG) systems based on renewable energy sources have rapidly developed. The DG systems are composed of micro source like fuel cells, photovoltaic (PV) cells, and wind power [1]–[7]. However, fuel cells and PV source are low-voltage sources to provide enough dc voltage for generating ac utility voltage. Although PV cells can connect in series to obtain sufficient dc voltage, it is difficult to avoid the shadow effect [8]–[10]. Thus, high step up dc–dc converters are usually used as the front-end converters to step from low voltage to high voltage which are required to have a large conversion ratio, high efficiency, and small volume [11]. Theoretically, the boost converter can provide a high step up voltage gain with an extremely high duty cycle [12]. In practice, the step-up voltage gain is limited by the effect of the power switch, rectifier diode, and the equivalent series resistance of the inductors and capacitors. Also, the extreme duty cycle operation may result in serious reverse-recovery and electromagnetic interference problems [13]. Some converters like the forward and flyback converters can adjust the turn ratio of the transformer to achieve a high step up voltage gain.

However, the main switch will suffer high voltage spike and high power dissipation caused by the leakage inductor of the transformer [14]. Although the non dissipative snubber circuits and active-clamp circuits can be employed, the cost is increased due to the extra power switch and high side driver [15]. To improve the conversion efficiency and achieve a high step up voltage gain, many step-up converters have been proposed [16]–[30]. A high step-up voltage gain can be achieved by the use of the switched-capacitor [16], [17] and voltage-lift [18]– [20] techniques. However, the switch will suffer high charged current and conduction loss. The converters use the coupled-inductor technique to achieve a high step-up gain [21]. However, the leakage inductor leads to a voltage spike on the main switch and affects the conversion efficiency. For this reason, the converters using a coupled inductor with an active-clamp circuit have been proposed [22], [23]. An integrated boost–flyback converter is presented in which the secondary side of the coupled inductor is used as a flyback converter [24], [25]. Thus, it can increase the voltage gain. Also, the energy of the leakage inductor is recycled to the output load directly, limiting the voltage spike on the main switch. Additionally, the voltage stress of the main switch can be adjusted by the turn ratio of the coupled inductor. To achieve a high step-up gain, it has been proposed that the secondary side of the coupled inductor can be used as flyback and forward converters [26], [27]. Also, several converters that combine output-voltage stacking to increase the voltage gain are proposed [28]. Additionally, a high step-up boost converter that uses multiple coupled inductors with output stacking has been proposed [29], [30]. To achieve high step-up voltage gain and high efficiency, this paper proposes a novel high step-up ratio and clamp-mode converter with pv. The proposed converter adds two capacitors and two diodes on the secondary side of the coupled inductor to achieve a high step-up voltage gain. The coupled inductor can charge two capacitors in parallel and discharge in series. However, the leakage inductor of the coupled inductor may cause high power loss and a high voltage spike on the switch. Thus, a passive clamping circuit is needed to clamp the voltage level of the main switch and to recycle the energy of the leakage inductor.

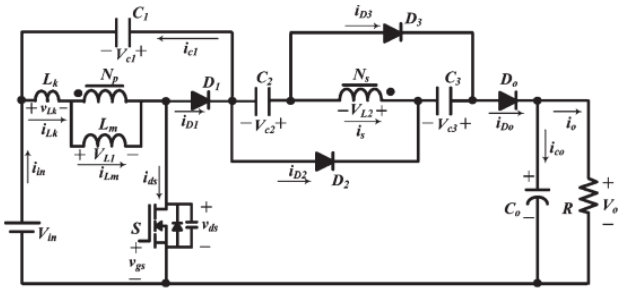

Fig. 1. Circuit configuration of the proposed converter.

OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

A. Derivation of the Proposed Converter

Fig. 1 shows the circuit topology of the proposed converter, which is composed of dc input voltage *Vin*, main switch *S*, coupled inductors *Np* and *Ns*, one clamp diode *D*1, clamp capacitor *C*1, two capacitors *C*2 and *C*3, two diodes *D*2 and *D*3, output diode *Do*, and output capacitor *Co*. The equivalent circuit model of the coupled inductor includes magnetizing inductor *Lm*, leakage inductor *Lk*, and an ideal transformer. The leakage inductor energy of the coupled inductor is recycled to capacitor *C*1, and thus, the voltage across the switch *S* can be clamped.

The voltage stress on the switch is reduced significantly. Thus, low conducting resistance *R*DS(ON) of the switch can be used. The original voltage-clamp circuit was first proposed in [11] to recycle the energy stored in the leakage inductor. Based on the topology, the proposed converter combines the concept of switched-capacitor and coupled-inductor techniques. The switched-capacitor technique in [17] has proposed that capacitors can be parallel charged and series discharged to achieve a high step-up gain. Based on the concept, the proposed converter puts capacitors *C*2 and *C*3 on the secondary side of the coupled inductor. Thus, capacitors *C*2 and *C*3 are charged in parallel and are discharged in series by the secondary side of the coupled inductor when the switch is turned off and turned on. Because the voltage across the capacitors can be adjusted by the turn ratio, the high step-up gain can be achieved significantly. Also, the voltage stress of the switch can be reduced. Compared to earlier studies [16]–[20], the parallel-charged current is not inrush. Thus, the proposed converter has low conduction loss. Moreover, the secondary-side leakage inductor of the coupled inductor can alleviate the reverse-recovery problem of diodes, and the loss can be reduced. In addition, the proposed converter adds capacitors *C*2 and *C*3 to achieve a high step-up gain without an additional winding stage of the coupled inductor. The coil is less than that of other coupled inductor converters. The main operating principle is that, when the switch is turned on, the coupled-inductor-induced voltage on the secondary side and magnetic inductor *Lm* is charged by *V*in. The induced voltage makes *V*in, *VC*1, *VC*2, and *VC*3 release energy to the output in series. The coupled inductor is used as a transformer in the forward converter. When the switch is turned off, the energy of magnetic inductor *Lm* is released via the secondary side of the coupled inductor to charge capacitors *C*2 and *C*3 in parallel. The coupled inductor is used as a transformer in the flyback converter.

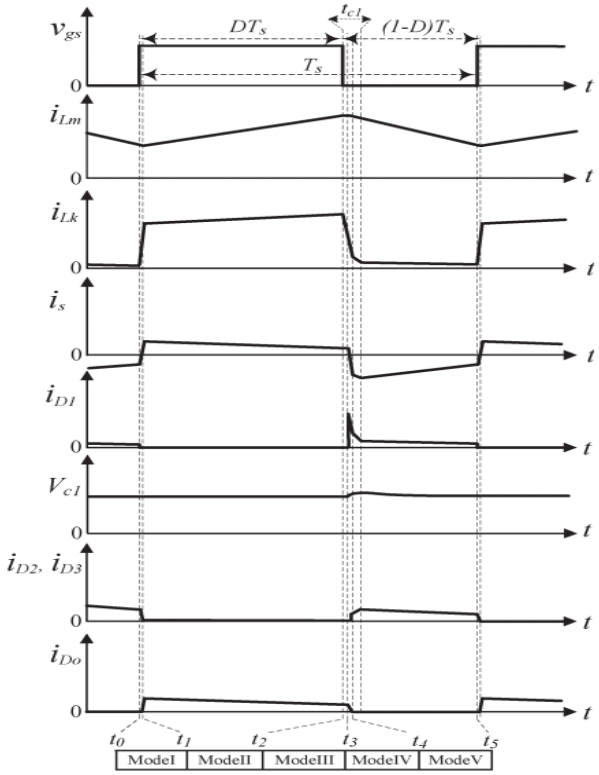

Fig 2 Some typical waveforms of the proposed converter at CCM operation

To simplify the circuit analysis, the following conditions are assumed.

1) Capacitors *C*1, *C*2, *C*3, and *Co* are large enough. Thus,*VC*1, *VC*2, *VC*3, and *Vo* are considered as constants in one switching period.

2) The power devices are ideal, but the parasitic capacitor of the power switch is considered.

3) The coupling coefficient of the coupled inductor *k* is equal to *Lm*/(*Lm* + *Lk*), and the turn ratio of the coupled inductor *n* is equal to *Ns*/*Np*. The proposed converter operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is analyzed as follows.

B. CCM Operation

This section presents the operation principle of the proposed converter. The following analysis contains the explanation of the power flow direction of each mode. In CCM operation, there are five operating modes in one switching period. Fig. 2 shows the typical waveforms, and Fig. 3 shows the current-flow path of each mode of the circuit. The operating modes are described as follows.

1) Mode I [*t*0,*t*1]: During this time interval, *S* is turned on. Diodes *D*1 and *Do* are turned off, and *D*2 and *D*3 are turned on. The current-flow path is shown in Fig. 3(a). The voltage equation on the leakage and magnetic inductors of the coupled inductor on the primary side is expressed as *V*in = *VLk* + *VLm*. The leakage inductor *Lk* starts to charge by *V*in. Due to the leakage inductor *Lk*, the secondary-side current *is* of the coupled inductor is decreased linearly. Output capacitor *Co* provides its energy to load *R*. When current *iD*2 becomes zero at *t* = *t*1, this operating mode ends.

2) Mode II [*t*1,*t*2]: During this time interval, *S* remains turned on. Diodes *D*1, *D*2, and *D*3 are turned off, and *Do* is turned on. The current-flow path is shown in Fig. 3(b). Magnetizing inductor *Lm* stores energy generated by dc source *V*in. Some of the energy of dc-source *V*in transfers to the secondary side via the coupled inductor. Thus, the induced voltage *VL*2 on the secondary side of the coupled inductor makes *V*in, *VC*1, *VC*2, and *VC*3, which are connected in series, discharge to high-voltage output capacitor *Co* and load *R*. This operating mode ends when switch *S* is turned off at *t* = *t*2.

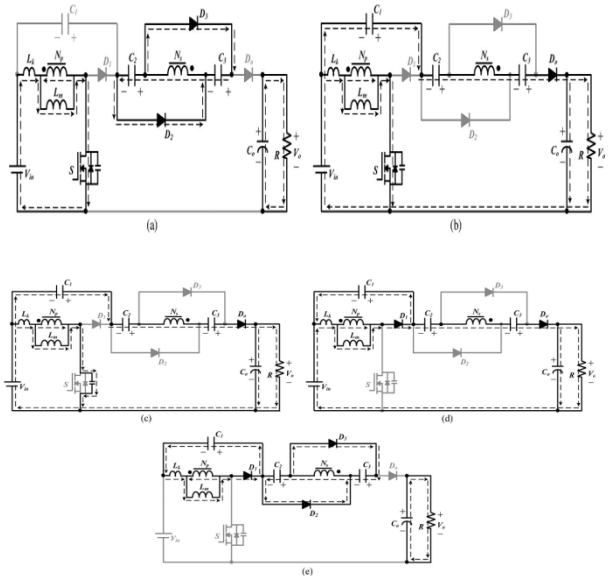

Fig. 3. Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

3) Mode III [*t*2,*t*3]: During this time interval, *S* is turned off. Diodes *D*1, *D*2, and *D*3 are turned off, and *Do* is turned on. The current-flow path is shown in Fig. 3(c). The energies of leakage inductor *Lk* and magnetizing inductor *Lm* charge the parasitic capacitor *C*ds of main switch *S*. Output capacitor *Co* provides its energy to load *R*. When the capacitor voltage *VC*1 is equal to *V*in + *V*ds at *t* = *t*3, diode *D*1 conducts, and this operating mode ends.

4) Mode IV [*t*3,*t*4]: During this time interval, *S* is turned off. Diodes *D*1 and *Do* are turned on, and *D*2 and *D*3 are turned off. The current-flow path is shown in Fig. 3(d). The energies of leakage inductor *Lk* and magnetizing inductor *Lm* charge clamp capacitor *C*1. The energy of leakage inductor *Lk* is recycled. Current *iLk* decreases quickly.

Secondary-side voltage *VL*2 of the coupled in ductor continues charging high-voltage output capacitor *Co* and load *R* in series until the secondary current of the coupled inductor *is* is equal to zero. Meanwhile, diodes *D*2 and *D*3 start to turn on. When *iDo* is equal to zero at $t = t4$, this operating mode ends.

5) Mode V [*t*4,*t*5]: During this time interval, *S* is turned off. Diodes *D*1, *D*2, and *D*3 are turned on, and *Do* is turned off. The current-flow path is shown in Fig. 3(e). Output capacitor *Co* is discharged to load *R*. The energies of leakage inductor *Lk* and magnetizing inductor *Lm* charge clamp capacitor *C*1. Magnetizing inductor *Lm* is released via the secondary side of the coupled inductor and charges capacitors *C*2 and *C*3. Thus, capacitors *C*2 and *C*3 are charged in parallel. As the energy of leak age inductor *Lk* charges capacitor *C*1, the current *iLk* decreases, and *is* increases gradually. This mode ends at $t = t\ 6$ when *S* is turned on at the beginning of the next switching period.

C. DCM Operation

To simplify the analysis of DCM operation, leakage inductor *Lk* of the coupled inductor is neglected. Fig. 4 shows the typical waveforms when the proposed converter operates in DCM, and Fig. 5 shows each mode of the operating stages. In this section, there are three modes, and the operating modes are described as follows.

1) Mode I [$t\ 0$,$t\ 1$]: During this time interval, *S* is turned on. The current-flow path is shown in Fig. 5(a). The magnetizing inductor *Lm* stores the energy from dc source *V*in. Thus, *iLm* increases linearly. Also, the energy of dc-source *V*in is transferred to the secondary side of the coupled inductor, which is connected with capacitors *C*2 and *C*3 in series to provide their energies to output capacitor *Co* and load *R*. This mode ends when *S* is turned off at $t = t1$.

2) Mode II [*t*1,*t*2]: During this time interval, *S* is turned off. The current-flow path is shown in Fig. 5(b). The energy of magnetizing inductor *Lm* transfers to capacitors *C*1, *C*2, and *C*3. Output capacitor *Co* provides its energy to load *R*. This mode ends when the energy stored in *Lm* is depleted at $t = t2$.

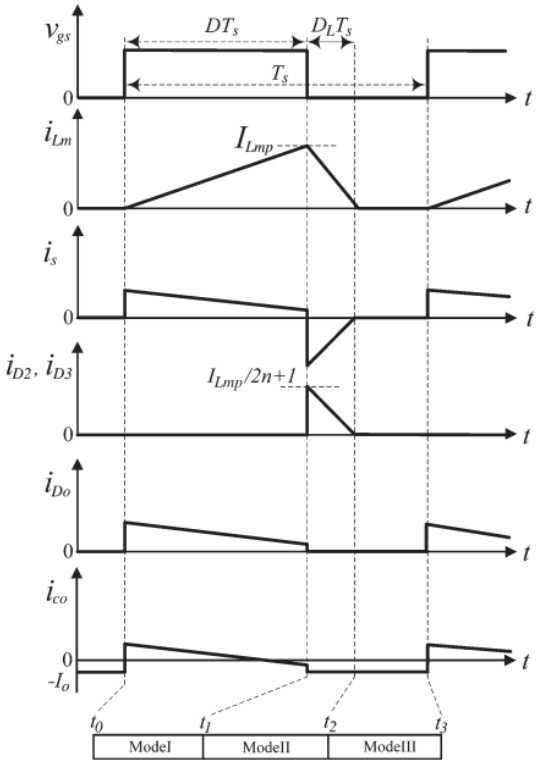

Fig. 4. Some typical waveforms of the proposed converter at DCM operation.

3) Mode III [*t*2,*t*3]: During this time interval, *S* remains turned off. The current-flow path is shown in Fig. 5(c). Since the energy stored in *Lm* is depleted, the energy stored in *Co* is discharged to load *R*. This mode ends when *S* is turned on at $t = t3$.

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STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

According to a previous work [11], the energy stored in the leakage inductor *Lk* of the coupled inductor is released to capacitor *C*1. The energy-released duty cycle *Dc*1 can be expressed as

$$D_{C1} = \frac{t_{C1}}{T_s} = \frac{2(1-D)}{n+1} \quad (1)$$

where *tC*1 is the time interval shown in Fig. 2. Because the times of modes I and III are significantly short, only modes II, IV, and V are considered in the steady-state analysis at CCM operation. In mode II, the following equations can be written based on Fig. 3(b):

$$u_{LK}^{II} = \frac{L_{K1}}{L_m+L_{K1}} V_{in} = (1-k)V_{in} \quad (2)$$

$$u_{L1}^{II} = \frac{L_{K1}}{L_m+L_{K1}} V_{in} = kV_{in} \quad (3)$$

$$u_{L2}^{II} = nu_{L1}^{II} = nkV_{in} \quad (4)$$

$$V_0 = V_{in} + V_{C1} + V_{C2} + u_{L2}^{II} + V_{C3} \quad (5)$$

By applying the voltage-second balance principle to the inductor, the following equations are given:

$$\int_0^{DT_s} u_{Lk}^{II} dt + \int_{DT_s}^{T_s} u_{Lk}^{V} dt = 0 \quad (6)$$

$$\int_0^{DT_s} u_{L1}^{II} dt \int_{DT_s}^{T_s} u_{L1}^{V} dt + = 0 \quad (7)$$

$$\int_0^{DT_s} u_{L2}^{II} dt + \int_{DT_s}^{T_s} u_{L2}^{V} dt = 0 \quad (8)$$

$$u_{LK}^{V} = -\frac{D(n+1)(1-k)}{2(1-D)} V_{in} \quad (9)$$

$$u_{L1}^{V} = -\frac{Dk}{1-D} V_{in} \quad (10)$$

$$u_{L2}^{V} = -\frac{nDk}{1-D} V_{in} \quad (11)$$

Substituting (1)–(4) into (6)–(8), the voltages in mode V can be derived. According to the definition of voltage direction, the voltages are expressed as

$$V_{C1} = -V_{LK}^{V} - V_{L1}^{V} = \frac{D}{1-D} V_{in} \frac{(1+k)+(1-k)n}{2} \quad (12)$$

$$V_{C2} = V_{C3} = u_{L2}^{V} = \frac{nDk}{1-D} \quad (13)$$

Also, capacitors *C*1, *C*2, and *C*3 are charged in mode V. The voltages across capacitors *C*1, *C*2, and *C*3 can be represented based on Fig. 3(e)

Substituting (4), (12), and (13) into (5), the voltage gain is obtained as

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{1+nk}{1-D} + \frac{D}{1-D} \cdot \frac{(k-1)+n(1+k)}{2} \quad (14)$$

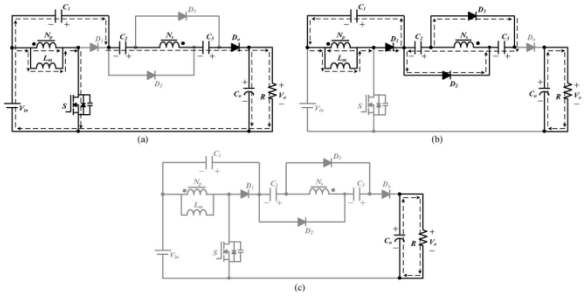


Fig. 5. Current-flow path of operating modes during one switching period at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.

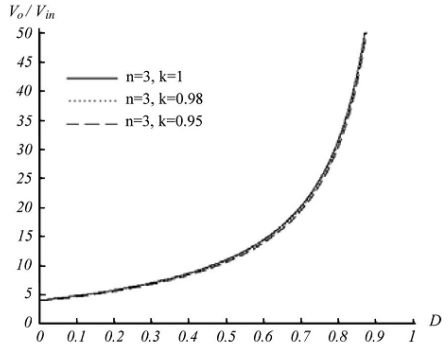


Fig. 6. Voltage gain versus duty ratio at CCM operation under $n = 3$ and various k's.

At $k = 1$, the ideal voltage gain is written as

$$M_{CCM} = \frac{1+n+nD}{1-D} \qquad (15)$$

The schematic of the voltage gain versus the duty ratio under various coupling coefficients of the coupled inductor is shown in Fig. 6. It shows that the voltage gain is not very sensitive to the coupling coefficient. Fig. 7 shows the voltage gain versus the duty ratio of the proposed converter compared with the converters in previous works [27] and [28] at CCM operation under $k = 1$ and $n = 3$. The voltage gain of the proposed converter is higher than those of the converters in [27] and [28]. According to the description of operating modes, voltage stresses on active switch S and diodes $D1$, $D2$, $D3$, and Do are given as

$$V_{ds} = \frac{1}{1-D}V_{in} = \frac{V_0+nV_{in}}{2n+1} \qquad (16)$$

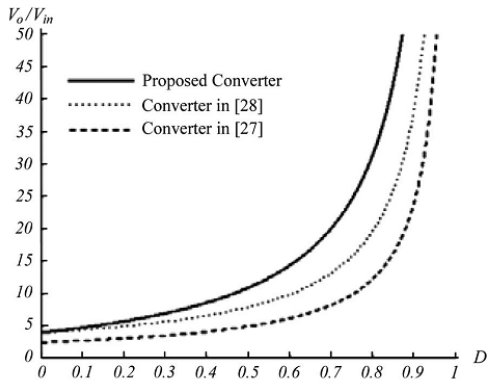


Fig. 7. Voltage gain versus duty ratio of the proposed converter and the converters in [27] and [28] at CCM operation under $n = 3$ and $k = 1$.

$$V_{D1} = \frac{1}{1-D}V_{in} = \frac{V_0+nV_{in}}{2n+1} \qquad (17)$$

$$V_{D2} = V_{D3} = V_{D0} = \frac{n}{1-D}V_{in} = \frac{n}{2n+1}(V_0 + nV_{in}) \qquad (18)$$

Equations (16)–(18) mean that, under the same voltage ratio, he voltage stresses can be adjusted by the turn ratio of the coupled inductor.

B. DCM Operation

In DCM operation, three modes are discussed. The typical waveforms are shown in Fig. 4. In mode I, switch S is turned on. Thus, the following equations can be formulated based on Fig. 5(a):

$$u_{L1}^{I} = V_{in} \qquad (19)$$

$$u_{L2}^{I} = nV_{in} \qquad (20)$$

$$V_0 = V_{in} + V_{c1} + V_{c2} + u_{L2}^{I} + V_{C3} \qquad (21)$$

The peak value of the magnetizing-inductor current is calculated as

$$I_{Lmp} = \frac{V_{in}}{L_m}DT_s \qquad (22)$$

In mode II, the following equation can be expressed based on Fig. 5(b):

$$u_{L1}^{II} = -V_{C1} \qquad (23)$$

$$u_{L2}^{II} = -V_{C2} = -V_{C3} \qquad (24)$$

In mode III, the following equation can be derived from Fig. 5(c):

$$u_{L1}^{III} = u_{L2}^{III} = 0 \qquad (25)$$

By applying the voltage-second balance principle to the coupled inductor, the following equations are given:

$$\int_0^{DT_s} u_{L1}^{I}\,dt + \int_{DT_s}^{(D+D_L)T_s} u_{L1}^{II}\,dt + \int_{(D+D_L)T_s}^{T_s} u_{L1}^{III}\,dt = 0 \qquad (26)$$

$$\int_0^{DT_S} u_{L2}^{I}\,dt + \int_{DT_s}^{(D+D_L)T_s} u_{L2}^{II}\,dt + \int_{(D+D_L)T_s}^{T_S} u_{L2}^{III}\,dt = 0 \qquad (27)$$

Substituting (19), (20), and (23)–(25) into (26) and (27), the voltages across the capacitors *C*1, *C*2, and *C*3 are obtained as follows:

$$V_{C1} = \frac{D}{D_L} V_{in} \qquad (28)$$

$$V_{C2} = V_{C3} = \frac{nD}{D_L} V_{in} \qquad (29)$$

Substituting (20), (28), and (29) into (21), the voltage gain is obtained as follows:

$$V_0 = [\frac{D}{D_L}(2n + 1) + (n + 1)]V_{in} \qquad (30)$$

According to (30), the duty cycle *DL* can be derived as

$$D_L = \frac{(1+2n)DV_{in}}{V_0-(1+n)V_{in}} \qquad (31)$$

From Fig. 4, the energy stored on capacitor *C*2 is fully released to capacitor *Co* and load *R* in the steady state. Also, the average current *IDo* is equal to *ID2*; thus, the average current of *iCo* is computed as

$$I_{C0} = I_{D0} - I_0 = I_{D2} - I_0 = \frac{1}{2} D_L \frac{L_{Lmp}}{2n+1} - I_0 \qquad (32)$$

Because *ICo* is equal to zero under the steady state, substituting (22) and (31) into (32) yields

$$\frac{D^2 V_{in}^2 T_s}{2[V_0-(1+n)V_n]L_m} = \frac{V_0}{R} \qquad (33)$$

Then, the normalized magnetizing-inductor time constant is defined as

$$\tau L_m = \frac{L_m}{RT_S} \frac{L_m f_s}{R} \qquad (34)$$

where *fs* is the switching frequency.

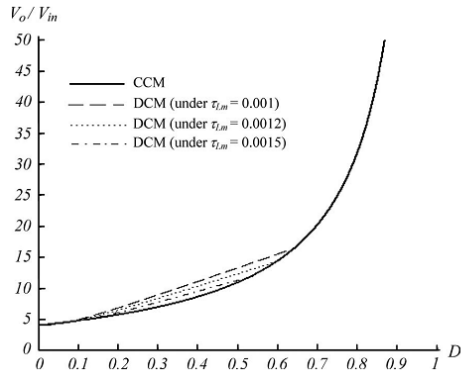


Fig 8 Voltage gain versus duty ratio at DCM operation under various *τLm* values and at CCM operation under *n* = 3 and *k* = 1.

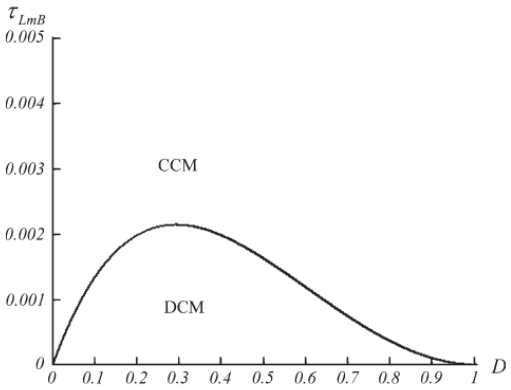


Fig 9 Boundary condition of the proposed converter under *n* = 3.

Substituting (34) into (33), the voltage gain is given by

$$M_{DCM} = \frac{V_0}{V_{in}} = \frac{1+n}{2} + \sqrt{\frac{(1+n)^2}{4} + \frac{D^2}{2\tau L_m}} \qquad (35)$$

The curve of the voltage gain, shown in Fig. 8, illustrates the voltage gain versus the duty ratio under various *τLm* values.

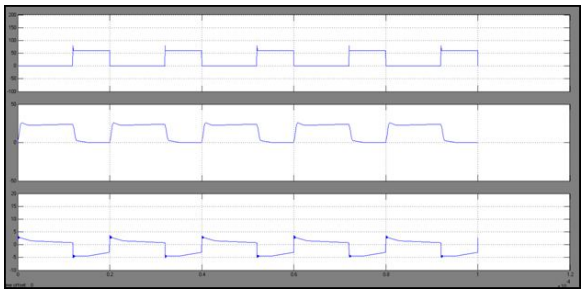
C. Boundary Operating Condition Between CCM and DCM

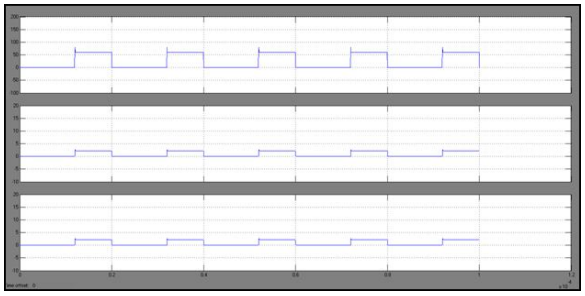
If the proposed converter is operated in boundary-

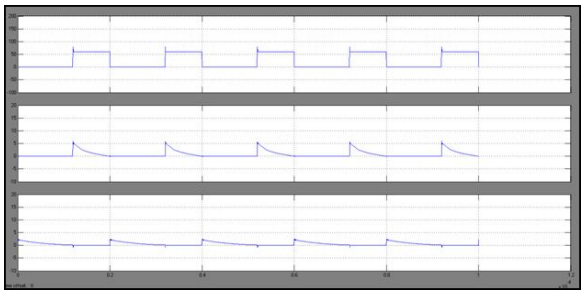
condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From (15) and (35), the boundary normalized magnetizing-inductor time constant τLmB can be derived as

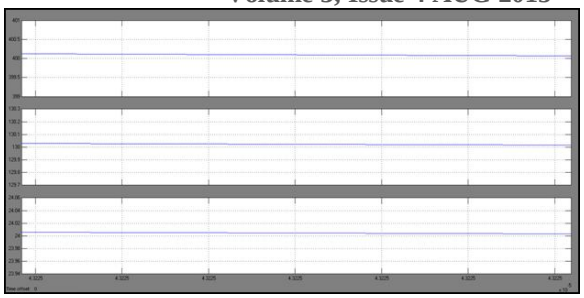
$$\tau LmB = \frac{D(1-D)^2}{2(1+2n)(1+n+nD)} \qquad (36)$$

The curve of τLmB versus the duty ratio of the proposed converter is shown in Fig. 9. If τLm is larger than τLmB, the proposed converter is operated in CCM operation.









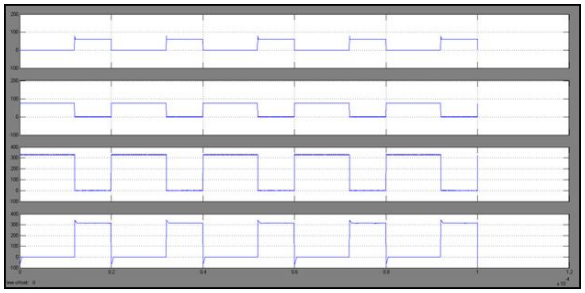


Fig 10 Experiment results under full-load *Po* = 200 W.

DESIGN AND EXPERIMENT OF THE PROPOSED CONVERTER

To verify the performance of the proposed converter, a proto type circuit is implemented in the laboratory. The specifications are as follows:

1) input dc voltage *V*in: 24 V;

2) output dc voltage *Vo*: 400 V;

3) maximum output power: 200 W;

4) switching frequency: 50 kHz;

5) MOSFET *S*: IRFB4410ZPBF;

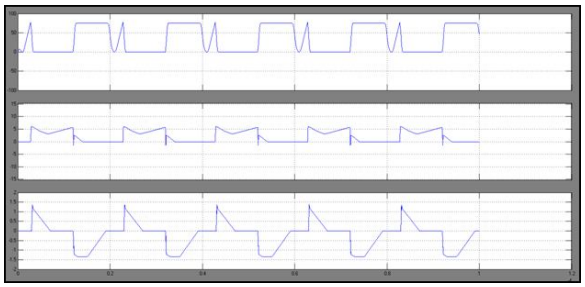
6) diodes *D*1: SBR20A100CTFP, *D2*/*D*3: DESI30, and *Do*: BYR29;

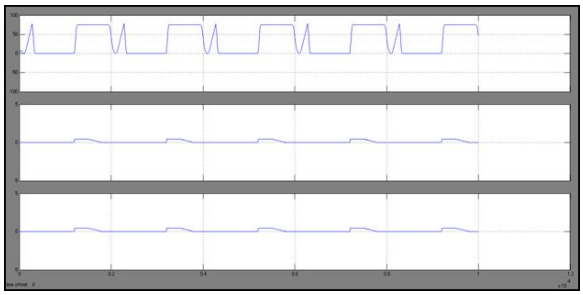
7) coupled inductor: ETD-59, core pc40, *Np* : *Ns* = 1 : 4,*Lm* = 48 μH, and *Lk* = 0.25 μH;

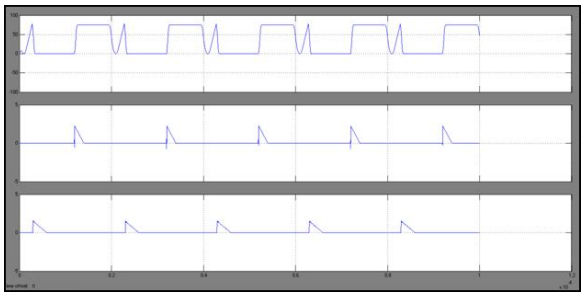
8) capacitors $C1$: 56 μF/100 V, $C2/C3$: 22 μF/200 V, and Co : 180 μF/450 V.

Fig. 10 shows the measured waveforms for full-load Po = 200 W and Vin = 24 V. The proposed converter is operated in CCM under the full-load condition.

The steady-state analysis







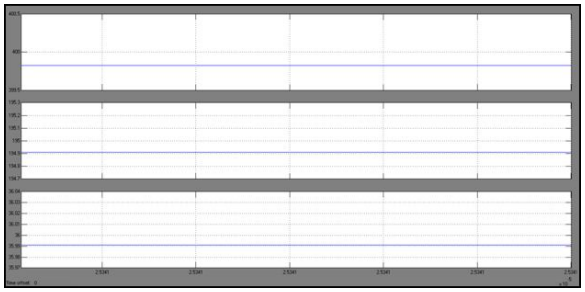


Fig 11 Experiment results under light-load Po = 30 W

can be demonstrated in the experimental results. In the measured waveforms, the voltage Vds across the main switch is clamped at approximately 84 V during the switch-off period. Therefore, a low-voltage-rated switch can be adopted to make the proposed converter reduce its conduction loss. In Fig. 10(a), the waveform of secondary current is of the coupled inductor shows that the proposed converter is operated in CCM because the current is not equal to zero when the switch is turned on. In Fig. 10(b), the waveforms of $iD2$ and $iD3$ show that capacitors $C2$ and $C3$ are charged in parallel, which verify the concept of the proposed converter. Fig. 10(c) shows that the energy of leakage inductor Lk is released to capacitor $C1$ through diode $D1$. Fig. 10(d) shows that $VC1$ and $VC2$ satisfied (12) and (13). In addition, output voltage Vo is consistent with (15). Fig. 10(e) shows the voltage stress of the main switch and diodes and demonstrates the consistency of (16)–(18). Fig. 11

Fig 12 Load variation between light-load Po = 30 W and full-load Po = 200 W.

shows the light-load waveforms. The output voltage is about 400 V, and the analysis of the DCM of the proposed converter is demonstrated. Fig. 12 shows the proposed converter under the output power variation between light-load 30 W and full-load 200 W.

CONCLUSION

This paper has proposed a novel high stride up dc–dc converter for DG frameworks with pv cells. By utilizing the capacitor charged as a part of parallel and released in arrangement by the coupled inductor, high stride up voltage increase and high productivity are accomplished. The consistent state examinations have been talked about in point of interest. At last, a 24-to 400-V 200-W model circuit of the proposed converter is put into operation in the research facility. The exploratory results have affirmed that high productivity and high stride up voltage addition can be accomplished. The top productivity is 95.88%. Also, the voltage on the primary switch is clasped at 84 V; along these lines, a switch with low voltage appraisals and low ON-state resistance RDS(ON) can be chose.

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